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Design:USB 1.1 SIE (Serial Interface Engine) Transmitter using VHDL

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Abstract
USB has become a popular interface for exchanging data between PC's and peripherals. An increasing number of portable peripherals are using the USB interface to communicate with the PC. The design and implementation of a synthesizable model of the USB 1.1 protocol engine is presented in this report The PHY is compatible with the USB 1.1 transceiver macrocell interface (UTMI) specification and the simulation test confirmed the successful operation of circuits for both full speed (12 Mbps) and low speed (1.5 Mbps) data transmission. the model is written completely in behavioral vhdl with a top down approach and the model was verified and validated.

Keywords
USB1.1 SIE, VHDL

I. Introduction
Universal Serial Bus (USB) has emerged as a result of the difficulties associated with thecost, configuration, and attachment of the peripheral devices in the personal computerenvironment. In short, USB creates a method of attaching, and accessing peripheraldevices that reduce overall cost, simplifies the attachment and configuration from theend-user perspective, and attempt to solve several technical issues associated with the old style peripherals.

II. Motivation
The motivation for the Universal Serial Bus (USB) comes from two interrelatedconsiderations:

III. Ease of use
The lack of flexibility in reconfiguring the PC has been acknowledged as the Achilles'heel to its further deployment. The combination of user-friendly graphical interfaces andthe hardware and software mechanisms associated with new-generation bus architectures have made computers less confrontational and easier to reconfigure.However, from the end user's point of view, the I/O interfaces of PC's, such asserial/parallel ports, keyboard/mouse/joystick interfaces, etc., do not have the attributesof plug-and-play.

IV. Port Expansion
The addition of external peripherals continues to be constrained by port availability. Thelack of a bi-directional, low-cost, low-to-mid speed peripheral bus has held back thecreative proliferation of peripherals such as telephone/fax/modem adapters, answeringmachines, scanners, PDA's, keyboards, mice, etc. Existing interconnects are optimizedto connect products for one or two ports. As each new function or capability is added tothe PC, a new interface has been defined to address this need.The USB is the answer to connectivity for the PC architecture. It is a fast, bidirectional,isochronous, low-cost, dynamically attachable serial interface that isconsistent with the requirements of the PC platform of today and tomorrow.

V. Objective of the thesis
This thesis describes the protocol used in USB 1.1 system's low-level interface. It alsodescribes the type of transactions and errors in USB transactions.The goal is to Designing of Protocol Engine (Serial Interface Engine) for the USBdevice . The design of SIE (Serial Interface Engine) is implemented in a VerilogHardware Description Language.

VI. overview of the task
The purpose of this thesis is to make a Verilog synthesizable model of USB 1.1 protocol
engine.

VII. Main Task
• Obtaining a complete functional description of the full system, based on the
Details given in the USB 1.1 standard specification.
• Analysing the variations of the Verilog model from the actual USB 1.1 spec
• Modelling the complete system in Verilog using the tool Model Sim.
• Simulation of the individual blocks and entire design with various test cases.
The guide for the design was the USB 1.1 standard specification. The implementeddesign has to be validated through testing. The behaviour of the model was validated withthe signals and timing details given with the specification.

VIII. Design of the system and tools used
The design was structured into different levels. It includes device transmitter and devicereceiver block, DPLL block, memory block, counter block. the total design was made easy with Mentor graphics HDL tool. A graphical user interface was provided to designthe various functional blocks and their descending level hierarchy along withinterconnecting the various blocks. so a great part of coding effort was reduced by theefficient usage of the tool to code the interface parts and the whole structure of thesystem.The various blocks designed were simulated individually using the ModelSim, which is apart of Mentor Graphics. The synthesizability of the model was checked by ISE toolpackage

A. Features
Features are categorized by the following benefits:

1. Easy to use for end user
- Single model for cabling and connectors
- Electrical details isolated from end user (e.g., bus terminations)
- Self-identifying peripherals, automatic mapping of function to driver, and configuration
- Dynamically attachable and reconfigurable peripherals

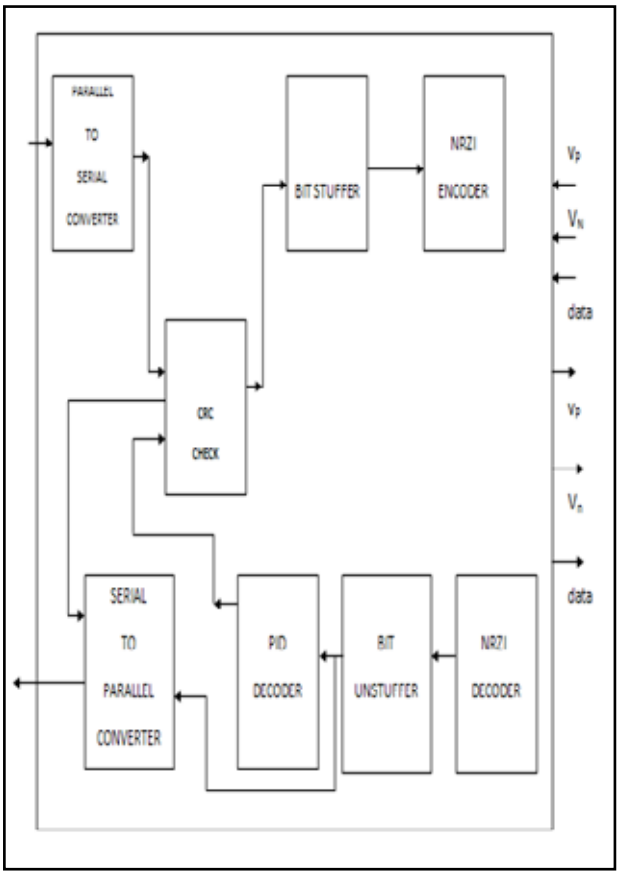

Fig. 1: Detailed Functional Block diagram

2. Wide range of workloads and applications

- Suitable for device bandwidths ranging from a few kb/s to several Mb/s
- Supports isochronous as well as asynchronous transfer types over the same set of wires
- Supports concurrent operation of many devices (multiple connections)
- Supports up to 127 physical devices
- Supports transfer of multiple data and message streams between the host and devices
- Allows compound devices (i.e., peripherals composed of many functions)
- Lower protocol overhead, resulting in high bus utilization

3. Isochronous bandwidth

- Guaranteed bandwidth and low latencies appropriate for telephony, audio, etc.
- Isochronous workload may use entire bus bandwidth

4. Flexibility

- Supports a wide range of packet sizes, which allows a range of device buffering options
- Allows a wide range of device data rates by accommodating packet buffer size and latencies
- Flow control for buffer handling is built into the protocol

5. Robustness

- Error handling/fault recovery mechanism is built into the protocol
- Dynamic insertion and removal of devices is identified in user-perceived real-time
- Supports identification of faulty devices

6. Synergy with PC industry

- Protocol is simple to implement and integrate
- Consistent with the PC plug-and-play architecture
- Leverages existing operating system interfaces

7. Low-cost implementation

- Low-cost subchannel at 1.5Mb/s
- Optimized for integration in peripheral and host hardware
- Suitable for development of low-cost peripherals
- Low-cost cables and connectors
- Uses commodity technologies

8. Upgrade path

- Architecture upgradeable to support multiple USB Host Controllers in a system

Result Obtained

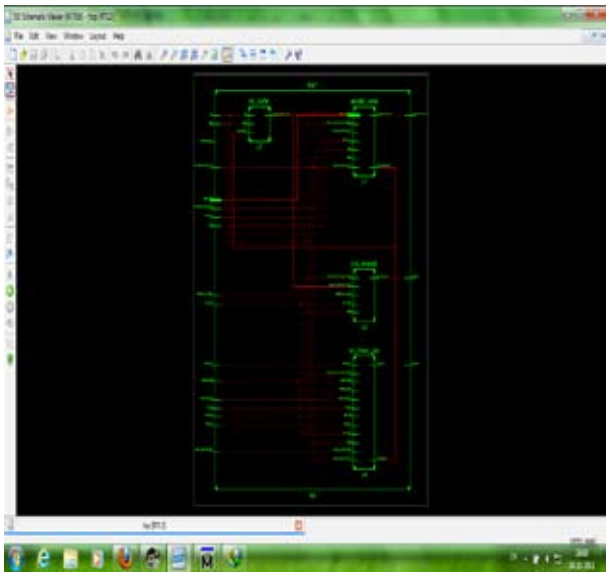

Fig. 2:

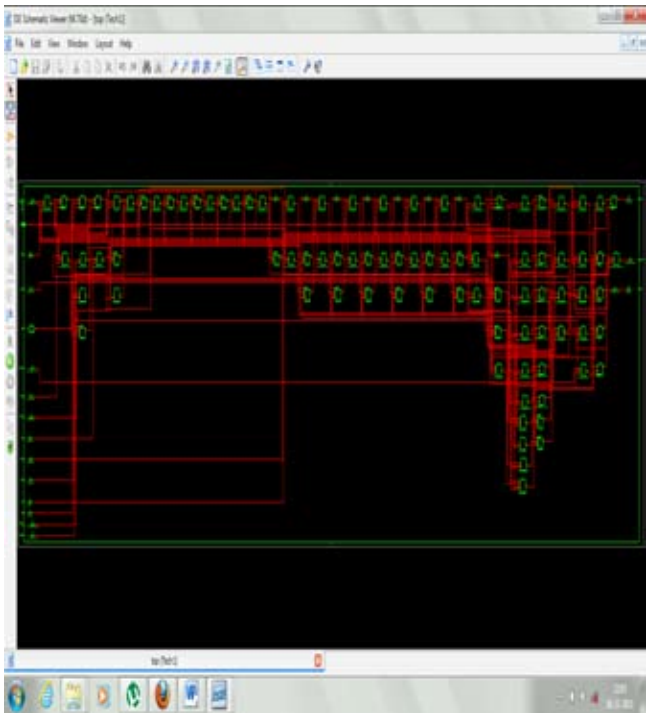

Fig. 3:

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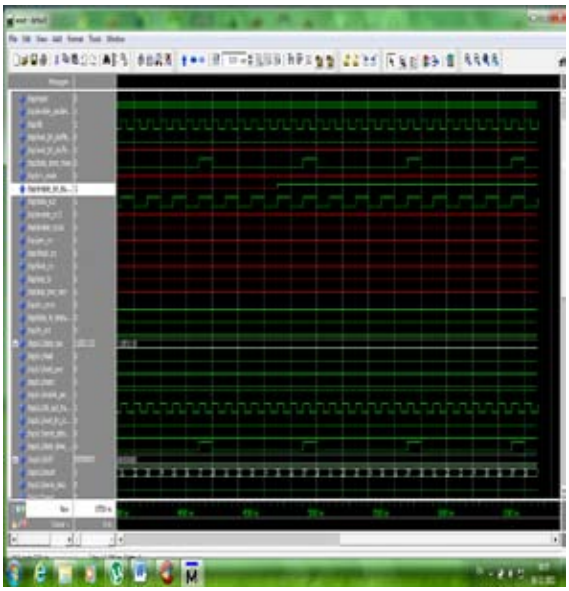

Fig. 4: Results of USB 1.1 SIE transmitter

References

[1] "Universal Serial Bus Specification 1.1", [Online] Availabe: http://:www.usb.org/developers/docs

[2] "Designing A Robust USB Serial Interface Engine (SIE)", [Online] Availabe: http://www.usb.org/developers/docs/Whitepapers

[3] "Cyclic Redundancy Checks in USB", [Online] Availabe: http://:www.usb.org/developers/docs/Whitepapers

[4] Don Anderson,"Universal Serial Bus System Architecture", Mindshare, Inc 1997.

[5] Sameer Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education Asia, 2001

[6] Mark Gordon Arnold, "Verilog Digital Computer Design: Algorithms to Hardware Design", Prentice Hall, 1999

[7] J. Bhasker by B.S PUBLICATION (2ND EDITION)

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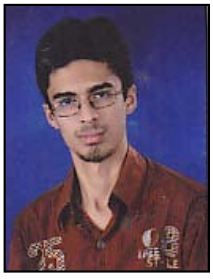

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