Abstract
ADC is required on microcontrollers to convert analog signals from transducers into digital signals so that various control functions can be performed. Analog to digital conversion takes time, this delay can be avoided by converting analog signal to digital repeatedly and updating ADC result register after T microseconds, where T equals the time that ADC takes to convert analog into digital. Whenever CPU needs to read analog value, it can read ADC result register without any delay.

Keywords
ADC, Microcontrollers, Acquisition Time, Conversion Time

I. Introduction
ADC determines the digital output number that is the equivalent of its input voltage. Different types of ADC circuits have been developed for various applications, FLASH converters are fast but of less accuracy, Dual ramp ADC are slow but of high accuracy, Successive approximation type ADC are of medium speed and medium accuracy. Successive approximation type ADC is most common in microcontrollers.

A. Sample and Hold
Analog voltage value should be sampled and kept constant then only it can be converted into digital value because most ADCs cannot convert changing voltage into digital value. To take sample of analog voltage there’s a Sample and Hold circuit made of switch and capacitor, when switch is closed it changes to Vs [1]. A simple sample and hold circuit is shown is fig. 1.

B. Acquisition and conversion time
There is always some series resistance in signal path so the capacitor voltage rises towards Vs exponentially.

\[ V_c = V_s \{ 1 - \exp(-t/RC) \} \]

\( V_c \) should be sufficiently close to Vs before switch is opened again. The time that \( V_c \) takes to reach value close to \( V_s \) is called acquisition time.

For good accuracy the error induced should be less than half of 1 LSB hence for 10bit conversion

\( V_c > (2^{10}/2^{11})V_s \) or \( V_c > 0.9995V_s \)

II. Study of ADC inside PIC16F877A
PIC16F877A is a popular microcontroller from Microchip, Successive approximation type ADC is there in PIC16F877A. Operation of ADC is governed by ADC clock of period TAD. A full 10bit conversion takes 12 TAD cycles; minimum clock period for correct operation is 1.6usec so fastest conversion time is 19.2usec [2]. Input model of analog to digital converter is shown in fig. 4 [4].
III. Acquisition Time

Acquisition time, \( T_{ac} \) = Amplifier settling time + Hold capacitance charging time + Temperature coefficient \( [3] \)

Amplifier settling time is fixed at 2usec\( [3] \), temperature coefficient can be neglected as its effect is slight and hold capacitor charging time = 7.6RC

Here, \( R = R_{ss} + R_{ic} + R_s \)

Taking \( R_s = 0, R_{ic} = 1\, Kohm, R_{ss} = 7\, Kohm \) at 5Volt

Charging time = 7.6(1k+7k) 120pF = 7.3usec

So Acquisition time = 7.3usec + 2usec = 9.3usec

Total time required = acquisition time + conversion time = 9.3usec + 19.2usec = 28.5usec \([1]\). Flowchart of analog to digital conversion is shown in Fig. 3.

CPU has to wait for 28.5usec to get converted digital value from the result register. This delay of 28.5usec can be avoided by introducing control logic for ADC. The function of this control logic is to start sampling the analog voltage and then wait for acquisition time and then start conversion and then for time equal to conversion time and finally latching the converted value into the result register and starting the same process again.

The result register will always have a digital output value so CPU can read the register anytime thus avoiding the delay of 28.5usec.

CPU can read converted value anytime so question is how old is that value? The result gets updated after every 28.5usec so for the worst case it can be 28.5usec old i.e. CPU reads result register just before it was going to be updated. This is acceptable in most of the cases.

IV. Control logic of ADC

The control logic for ADC can be made with a Timer and few logic gates. Taking 8 bit timer and clock period = 0.2usec as an example, the timer will overflow after 255 clock cycles (i.e. 51 usec)

So when timer = 0 switch of sample and hold circuit is closed.

When timer = 47 (9.4usec) switch open and conversion starts.

When timer = 143 (28.6usec) latch converted value into result register and reset timer.

Flowchart of 8bit timer inside control logic is shown in fig. 5.

If more than 1 analog input is to be converted value then control logic will first select the input and then converted value will be saved in R1 then second analog input will be selected and its converted value will be stored in R2 and so on. so if 4 analog inputs are taken each of them will get updated after 4x28.5usec. Figure 6 shows the control logic of ADC controlling different stages of ADC.

Example to see benefits of this system Suppose CPU takes 100usec to perform control functions so total time to read analog voltage and execute control functions is 100usec + 28.5usec = 128.5usec but now CPU can read converted value anytime without any delay so total time is now 100usec only. Fig. 7, shows the flowchart of simple program which uses analog to digital conversion to read transducers and performs some control functions.

V. Conclusion

This paper presents the introduction of control logic for ADC on microcontrollers to avoid the time delay of converting analog voltage into digital value, the control logic for ADC works on parallel with CPU so this control logic takes care of everything related to ADC while CPU can continue with other important work PIC16F877A is used as another example to study delay values in ADC. This technique can be used for all microcontrollers and even for ADC IC’s like AD0801 etc.
Fig. 6: Block Diagram of ADC with Control Logic

Fig. 7: Flowchart of an Example Program

References


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