# Half Bridge ZVS DC-DC Converter with DCS **PWM Active Clamp Technique**

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#### **Abstract**

Half Bridge (HB) DC-DC converter is an attractive topology for middle power level applications owing to its simplicity. This paper presents a new control scheme, to be known as duty-cycle shifted PWM (DCS PWM) control, is proposed and applied to the conventional HB dc-dc converters to achieve ZVS for one of the two switches without adding extra components and without adding asymmetric penalties of the complementary control. The concept of this new control scheme is shifting one of the two symmetric PWM driving signals close to the other, such that ZVS may be achieved for the lagging switch due to the shortened resonant interval. Moreover, based on the DCS PWM control, an active clamp branch comprising an auxiliary switch and a diode is added across the isolation transformer primary winding in the half bridge converter to achieve ZVS for the other main switch by utilizing energy stored in the transformer leakage inductance. Moreover, the auxiliary switch also operates at ZVS and ZCS conditions. In addition, the proposed topology with DCS PWM control eliminates the ringing resulting from the oscillation between the transformer leakage inductance and the switches junction capacitances during the off-time period. Therefore, the proposed converter has a potential to operate at higher efficiencies and switching frequencies.

#### **Keywords**

Duty-Cycle-Shifted (DCS), Half Bridge (HB), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Pulse-Width Modulated (PWM), Zero-Current Switching (ZCS), Zero-Voltage Switching (ZVS)

#### I. Introduction

The new techniques for high frequency DC–DC conversion have been proposed to reduce component stresses and switching losses while achieving high power density and improved performance. Among them, the phase-shifted Zero-Voltage-Switching (ZVS) full bridge is one of the most attractive techniques since it allows all switches to operate at ZVS by utilizing transformer leakage inductance and metal oxide semiconductor field effect transistors' (MOSFETs) junction capacitance without adding an auxiliary switch. However, the complexity of the full-bridge is almost highest among the conventional topologies due to its large switch count and complicated control and driving. Activeclamp forward topology is another typical example to successfully realize ZVS for the switches by utilizing the leakage inductance, magnetizing inductance and junction capacitance. However, the topology of the converter is asymmetric and the energy-delivery is unidirectional. In other words, voltage and current stresses are unevenly distributed, which results in the individual switch and rectifier stresses being higher compared to symmetric half-bridge and full-bridge converters. This disadvantage limits power level of the active-clamp forward topology applications. In addition, dc bias of magnetizing current may exist in the transformer.

Half Bridge (HB) DC–DC converter is an attractive topology for

middle power level applications owing to its simplicity. There are two conventional control schemes for the HB DC-DC converter, namely, symmetric control and asymmetric (complimentary) control. The main drawback of the conventional symmetric control is that both primary switches in the converter operate at hard switching condition. Moreover, during the off-time period of two switches, the oscillation between the transformer leakage inductance and junction capacitance of the switches results in energy dissipation and Electromagnetic Interference (EMI) emissions due to reverse recovery of MOSFETs body diodes. To suppress the ringing, resistive snubbers are usually added. As a result, energy in the transformer leakage inductance is significantly dissipated in snubbers. Therefore, the symmetriccontrol half bridge is not a good candidate for high switching frequency power conversion. The asymmetric (complementary) control was proposed to achieve ZVS operation for HB switches. Two drive signals are complementarily generated and applied to high side and low side switches. Thus, the two HB switches may be turned on at ZVS conditions owing to the fact that the transformer primary current charges and discharges the Junction capacitance. However, asymmetric stresses distribution on the corresponding components may occur due to the asymmetric duty cycle distribution for the two primary Switches. In other words, current stresses in the two primary switches are not identical and voltage and current stresses on secondary rectifiers are not equal. As a result, diodes or synchronous rectifiers with higher voltage rating are needed at the penalty of degrading the performance and efficiency of the rectifier stage. Furthermore, the dc gain ratio of the converter is nonlinear, thus higher duty cycle variation is needed for the same input voltage variation in comparison with symmetric PWM control scheme, which makes the converter operate further beyond the optimum operating point at high input voltage Therefore, the complementary (asymmetric) PWM control is more suitable for applications where the input voltage is fixed. As a solution to reduce the duty cycle variation for wide input voltage range, an asymmetric transformer turns ratio together with integrated-magnetic structure was proposed. such that rectifiers with lower withstanding voltage may be used to improve the

A new control scheme, to be known as duty-cycle shifted PWM (DCS PWM) control, is proposed and applied to the conventional HB dc–dc converters to achieve ZVS for one of the two switches without adding extra components and without adding asymmetric penalties of the complementary control. The concept of this new control scheme is shifting one of the two symmetric PWM driving signals close to the other, such that ZVS may be achieved for the lagging switch due to the shortened resonant interval. Unlike the asymmetric control, the width of the duty cycle for the two switches is kept equal, such that all corresponding components work at the conditions with even stresses as the case in the symmetric control scheme. Moreover, based on the DCS PWM control, a new half-bridge topology is proposed to achieve ZVS for the other switch and auxiliary switch by adding an auxiliary

switch and diode in the conventional half bridge. ZVS for the other switch is achieved by utilizing the energy trapped in the leakage inductance. In addition, the proposed topology with DCS PWM control eliminates the ringing resulting from the oscillation between the transformer leakage inductance and the switches junction capacitances during the off-time period. Therefore, the proposed converter has a potential to operate at higher efficiencies and switching frequencies.

## II. Conventional Half Bridge Converter Principle of Operation

Please fig. 1 shows the half-bridge dc-dc converter. The ideal waveforms for the symmetric PWM control is sketched in fig. 2, where Lk, is the leakage inductance; ip,im are the transformer primary-side input and magnetizing currents, respectively; and  $i_{D1}$  is the forward current through rectifier diode D<sub>1</sub> Besides the hard switching, conventional symmetric PWM control has transformer-leakage inductance related disadvantages. During the off-time period when both switches are off, the energy stored in the transformer leakage inductance may be recycled to primary dc bus through body diodes of MOSFETs. However, because of reverse recovery current of body diodes, the oscillation between the transformer leakage inductance and the MOSFETs' junction capacitance is significant on the primary side. To suppress the ringing, usually, snubber circuits are necessarily added, but losses dissipated in the snubber become dramatically large, especially at high input current and high switching frequencies.

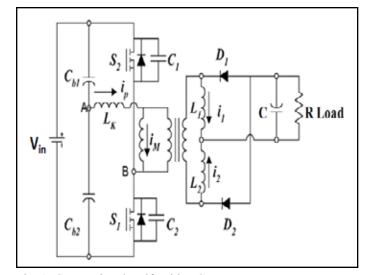


Fig. 1: Conventional Half Bridge Converter

To simplify the analysis of operation, components are considered ideal except otherwise indicated. The main operation modes are described as follows.

Mode 1 ( $t < t_1$ ): Initially  $S_1$  is conducting, and the input power is delivered to the output. is charged and freewheels through.

Mode 2  $(t_1 < t < t_2)$ :  $S_1$  is turned off at  $t = t_1$ , causing the primary current to charge C<sub>2</sub> and discharge C<sub>1</sub>. During the interval, the reflected secondary inductor current dominates the primary current i1. Thus, C<sub>1</sub> may be discharged to zero at wide load range, which means wide ZVS range can be achieved for S<sub>2</sub>.

Mode 3 ( $t_2 < t < t_3$ ): When the voltage across  $\tilde{C}_1$  is discharged to zero at  $t=t_2$ , the body diode of  $S_2$  conducts to carry the current, which provides ZVS condition for switch S<sub>2</sub>. During this period, leakage inductance is reset and secondary current i, and i, freewheel through  $D_1$  and  $D_2$ , respectively.

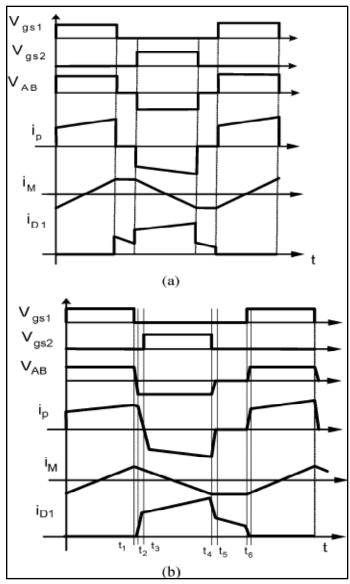


Fig. 2: Waveforms Comparison of the Half Bridge DC-DC converter: Symmetric PWM Control and (b) DCS PWM Control

Mode 4 ( $t_3 < t < t_4$ ):  $S_2$  is turned on with ZVS at  $t = t_3$ ; the primary current decreases to zero and then becomes negative. When the negative peak current equals to the reflected L<sub>2</sub> current, the diode D<sub>2</sub> is blocked and the converter starts to deliver power to the output. The inductor L<sub>2</sub> is charged and inductor current continues to freewheel.

Mode 5 ( $t_4 < t < t_5$ ):  $S_2$  is turned off at  $t = t_4$ , causing the primary current ip to charge  $C_1$  and discharge  $C_2$ . When the secondary D<sub>1</sub> and D<sub>2</sub> start to freewheel, leakage inductance and junction capacitance of switches  $S_{12}$  and  $S_{2}$  start to oscillate on the primary side. During the interval, body diodes may be involved, which worsens the ringing and results in reverse recovery losses.

Mode 6 ( $t_5 < t < t_6$ ): The oscillation comes to the end with equal voltage across switches  $S_1$  and  $S_2$ . On the secondary side,  $L_1$  and  $L_2$  keep freewheeling. At  $t = t_6$ ,  $S_1$  is turned on again going back to Mode 1.

# **B. DCS PWM Control Scheme**

Fig. 2, shows the key waveforms of the half-bridge converter with the proposed DCS PWM control. Based on symmetric PWM control, driving signal is shifted left such that the rising edge is close to the falling edge of driving signal. When is turned off, the transformer primary current charges the junction capacitance of switch and discharges the junction capacitance of switch. After the voltage across drain-to-source of drops to zero, the body diode of conducts to carry the current. During the body diode conduction period, may be turned on at zero-voltage switching. No ringing occurs during the transition period.

Fig. 3 shows a possible modulation approaches for the realization of DCS PWM control. Where, Vsaw is the SAW carrier waveform for modulation; VC and – VC are control voltages derived from the controller. By modulating VC and – VC, driving signals for S<sub>4</sub> and S<sub>2</sub> can be generated, respectively. Because the falling time of the saw waveform is short, the falling edge of  $S_1$  is always close to the rising edge of S<sub>2</sub>, which provide a possibility of ZVS for S<sub>2</sub>.

#### **C. Simulation Results**

The simulation is done using matlab simulink and the results are presented here. The circuit of ZVS HB DC to DC converter is shown in fig 3.a. Driving pulses for the MOSFET s are shown in fig3.b. The voltage across S1 is shown in fig3.c. Voltage across S2 is shown in fig 3.d. Voltage across the primary of the transformer is shown in fig 3.e. Voltage across secondary of the transformer is shown in fig 3.f. and output voltage is shown in fig 3.g.

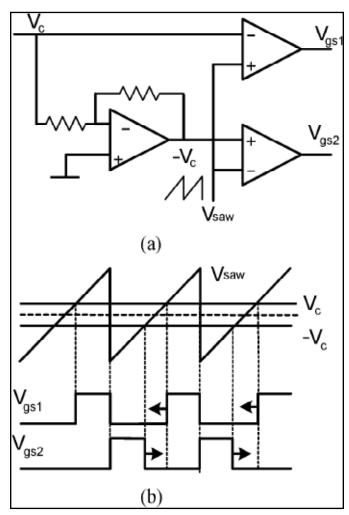


Fig. 3: DCS PWM Modulation Scheme: (a) Modulation Circuits and (b) Key Waveforms

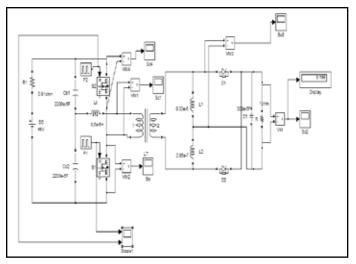


Fig. 3: (a). Simulink circuit diagram of ZVS half bridge DC-DC Converter

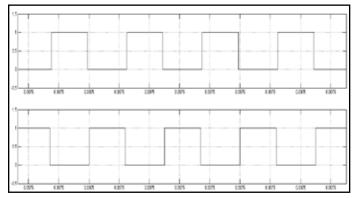


Fig. 3.b. Gate signal of switches S<sub>1</sub> & S<sub>2</sub>

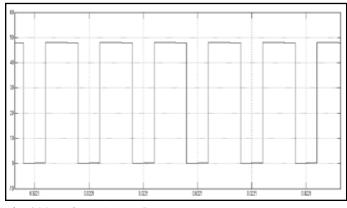


Fig. 3(c). Voltage Across S<sub>4</sub>

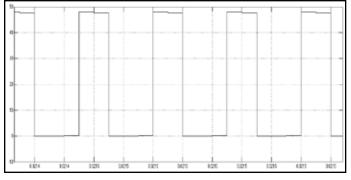


Fig. 3(d): Voltage Across S<sub>2</sub>

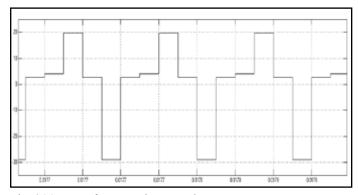


Fig. 3(e): Transformer Primary Voltage

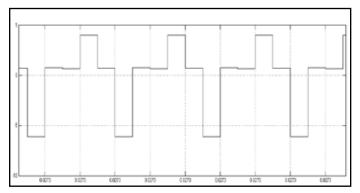


Fig. 3(f): Transformer Secondary Side Voltage

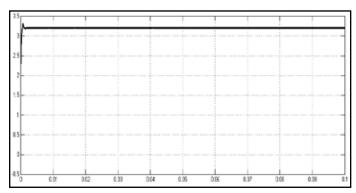


Fig. 3(g): Output Voltage (V)

# III. Modified DCS PWM HB DC-DC Converter

As described in section II, ZVS of switch S<sub>2</sub> is achieved by using the DCS PWM control scheme. However, switch  $\mathbf{S}_1$  still operates at hard-switching condition. To achieve ZVS for S<sub>1</sub>, a modified DCS ZVS HB DC-DC converter is proposed as shown in fig. 4. Where  $S_1$  and  $S_2$  are two main switches and an auxiliary branch consists of S<sub>3</sub> and D<sub>3</sub>. It is noted that the switch S<sub>3</sub> is grounded instead of floating in fig. 4, and thus the drive circuitry becomes simple and reliable. The key waveforms are shown in fig. 4.(b), where drive signal of the switch S<sub>2</sub> is shifted left close to the falling edge of  $S_1$  driving signal so that  $\tilde{S}_2$  may achieve ZVS. During the on time of the switch S<sub>2</sub>, switch S<sub>3</sub> turns on with ZVZCS. The transformer leakage inductance current freewheels through the auxiliary branch when the S<sub>2</sub> switch turns off. Later on the S<sub>3</sub> switch turns off, and the leakage inductance energy is released to achieve ZVS for the switch S<sub>1</sub>.

#### A. Principal of Operation

To simplify the analysis of operation, components are considered ideal except otherwise indicated. The main equivalent circuits for main operational modes are shown in fig. 5.

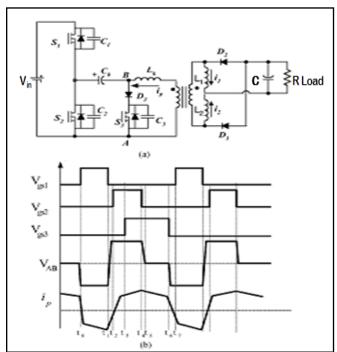
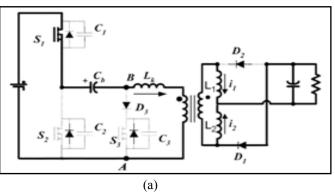
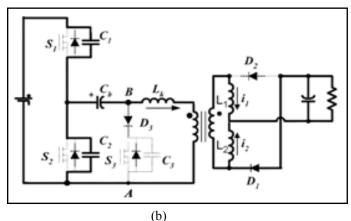
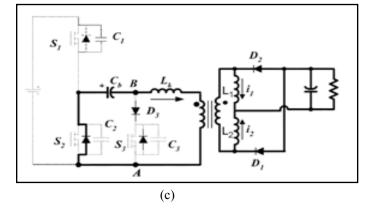
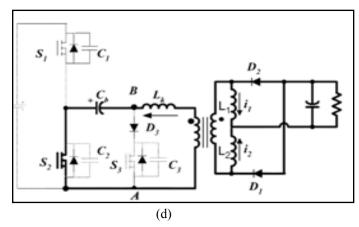


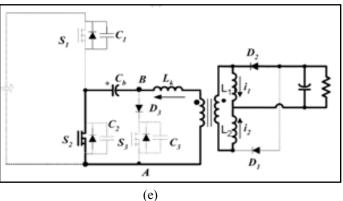
Fig. 4(a): Modified DCS ZVS HB DC-DC Converter

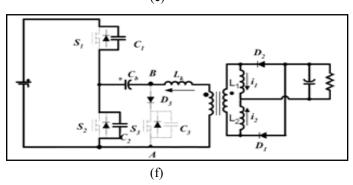


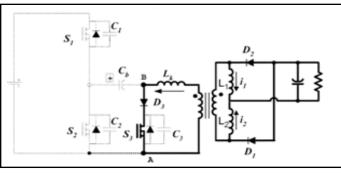


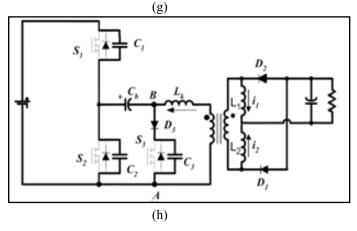












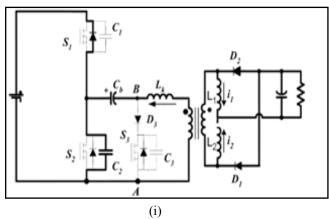


Fig. 5: Operation Modes of the Modified DCS HB DC–DC Converter (Mode 1–Mode 9)

Mode  $1(t_0 < t < t_2)$ : At  $t = t_0$ , turns on with ZVS. During the interval, the transformer primary current ip was negative, and the secondary side diode D2 was reverse-biased.

Mode  $2(t_1 < t < t_2)$ : At  $t = t_1$ , turns off causing the  $i_p$  current to charge  $C_1$  and discharge  $C_2$ .

Mode  $3(t_1 \le t \le t_2)$ : When the voltage across  $C_2$  is discharged to zero, the body diode of  $S_2$  conducts to carry the current, which provides ZVS condition for the switch  $S_2$ . During this subinterval, the secondary side current  $i_1$  and  $i_2$  freewheel through  $D_2$  and  $D_1$ , respectively.

Mode  $4(t_2 < t < t_3)$ :  $D_2 S_1$  is turned on with ZVS at  $t = t_2$ , which causes the transformer leakage inductance current to be, reset to zero and reverse-charged while the output inductor currents keep freewheeling.

Mode 5 ( $t_2 < t < t_4$ ):  $D_2$  When the primary transformer current reaches the reflected current of  $i_2$ , diode  $D_1$  is blocked and the inductor  $L_2$  is charged. At  $t=t_3$ , the switch  $S_3$  turns on with ZCS, because  $D_3$  is reverse-biased and no current goes through  $S_3$  until  $S_2$  is turned off.

Mode  $6(t_4 < t < t_5)$ :  $D_2$  At  $t=t_4$ ,  $S_2$  is turned off, and the primary transformer current discharges  $C_1$  while charging  $C_2$ .

Mode  $7(t_5 < t < t_6)$ :  $D_2$  At  $t=t_5$ , the voltage across  $C_2$  is charged to the voltage across the capacitor  $C_b$ , and then the leakage inductance current flows through  $D_3$  and  $S_3$ . During this interval, the leakage inductance current freewheels through  $D_3$  and  $S_3$  such that the energy in the leakage inductance is trapped. On the secondary side, inductor  $L_1$  and  $L_2$  currents freewheel through  $D_2$  and  $D_1$ , respectively.

Mode  $8(t_6 < t < t_7)$ :  $D_2$  At  $t=t_6$ ,  $S_3$  is turned off, causing  $C_2$  and  $C_3$  to be charged and  $C_1$  to be discharged by leakage inductance current.

Mode  $9(t_6 < t < t_7)$ : When the voltage across  $C_1$  is discharged to zero, the body diode of  $S_1$  conducts to recycle the energy in the transformer leakage inductance and offer a ZVS condition for switch  $S_1$ .

## **B. Simulation Results**

The simulation is done using matlab simulink and the results are presented here. The simulink circuit of a modified DCS ZVS HB dc-dc converter is shown in fig. 6(a). The voltage across  $S_1$  and its gate pulses are shown in fig. 6(b). The voltage across  $S_2$  and its gate pulses are shown in fig. 6(c). The voltage across  $S_3$  and its gate pulses are shown in fig. 6(d). The voltage across the primary of the transformer is shown in fig. 6(e). The voltage across secondary of the transformer is shown in fig. 6(f). The output voltage waveform is shown in fig. 6(g).

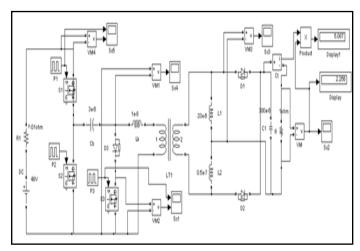


Fig. 6(a): Simulink Circuit of a Modified DCS ZVS HB DC-DC Converter

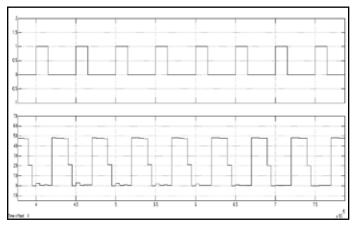


Fig. 6(b): Vgs and Vds Voltage Across S<sub>1</sub>

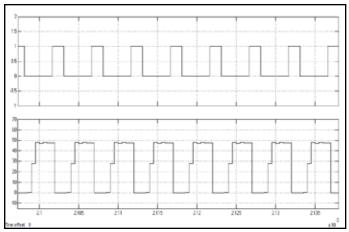


Fig. 6(c): Vgs and Vds Voltage Across S<sub>2</sub>

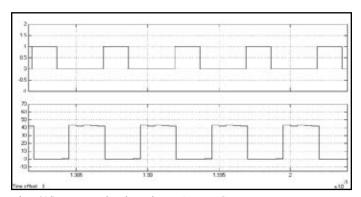


Fig. 6(d): Vgs and Vds Voltage Across S<sub>3</sub>

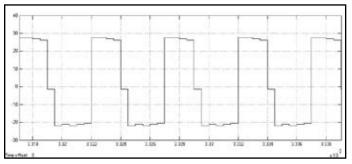


Fig. 6(e): Transformer Primary Voltage

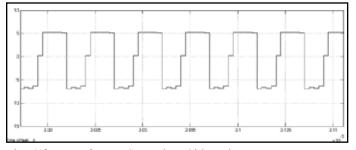


Fig. 6(f): Transformer Secondary Side Voltage

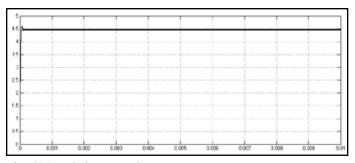


Fig. 6(g): DC Output Voltage

### **IV Conclusion**

A simple and effective PWM control method known as "dutycycle-shifted PWM" (DCS PWM) was proposed to reduce switching losses and transformer-leakage-inductance-related losses in half-bridge dc-dc converters. By employing the proposed DCS PWM control scheme, ZVS is achieved for one of the two switches without adding extra components and without asymmetric penalties of the complementary control. Based on the DCS PWM control scheme, two ZVS half-bridge topologies are presented and analyzed. Simulation results verify that all switches in the converters operate at soft switching such that switching losses are significantly reduced. Furthermore, the energy stored in the transformer leakage inductance is recycled to the input dc bus and utilized for ZVS operation of the switches instead of being dissipated in snubbers. Therefore, switching-frequencyrelated losses are significantly reduced, which provides converters with the potential to operate at higher frequencies and higher efficiencies. The proposed DCS PWM control and ZVS halfbridge topologies may also be used for high-voltage-input dc-dc applications.

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