Comparison Between Various Types of Adder Topologies

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Abstract
Adders are one of the most widely digital components in the digital integrated circuit design and are the necessary part of Digital Signal Processing (DSP) applications. With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them. In this paper, the design of various adders such as Ripple Carry Adder, Carry Skip Adder, Carry Increment Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Bypass Adder are discussed and are compared on the basis of their performance parameters such as area, delay and power distribution.

Keywords
Carry Bypass Adder, Carry Increment Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Skip Adder, Ripple Carry Adder.

I. Introduction

Arithmetic unit are the essential blocks of digital systems such as Digital Signal Processor (DSP), micro processors, micro controllers, and other data processing units. Adders become a critical hardware unit for the efficient implementation of arithmetic unit. In many arithmetic applications and other kinds of applications, adders are not only in the arithmetic logic unit, but also in other parts of processor. Addition operation can also be used in complement operations (1's, 2's, and so on), encoding, decoding and so on. In general, addition is a process which involves two numbers which are added and carry will be generated. The addition operations will result in sum value and carry value. All complex adder architectures are constructed from its basic building blocks such as Half Adder (HA) and Full Adder (FA). In this paper, the performance parameters of various adders are compared. The rest of the paper is organised as follows:
Section I deals with the introduction about adders. In section II, the architectures and the features of various adders are discussed. And section III deals with the comparison between various performance parameters of adders.

II. Adders

The design of various adders such as Ripple Carry Adder (RCA), Carry Skip Adder (CSkA), Carry Increment Adder (CIA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSlA) and Carry Bypass Adder (CBA) are discussed below. The each and every adder is named based on the propagation of carry between the stages.

A. Ripple Carry Adder

Ripple Carry Adder (RCA) is a basic adder which works on basic addition principle [1]. The architecture of RCA is shown in fig. 1.

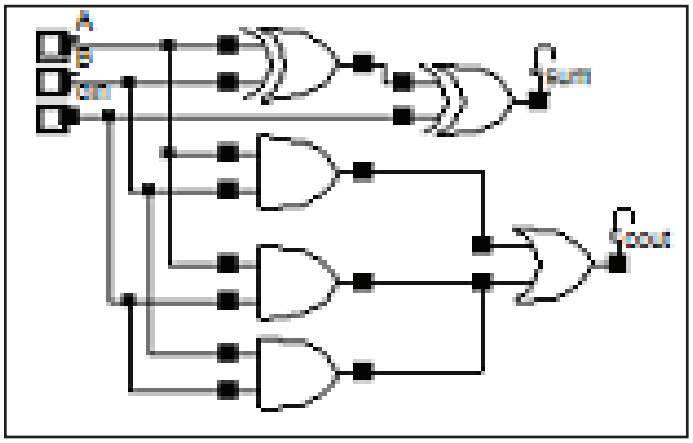

Fig. 1(a): Full Adder Design

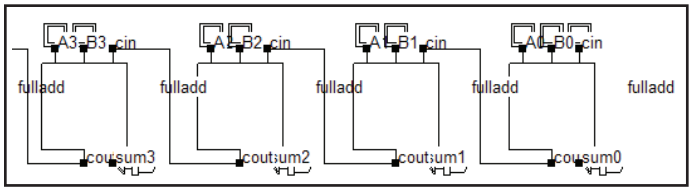

Fig. 1(b): Design of Ripple Carry Adder

RCA contains series structure of Full Adders (FA); each FA is used to add two bits along with carry bit.
The carry generated from each full adder is given to next full adder and so on. Hence, the carry is propagated in a serial computation [1]. Hence, delay is more as the number of bits is increased in RCA.

B. Carry Skip Adder

As the name indicates, Carry Skip Adder (CSkA) uses skip logic in the propagation of carry [1]. It is designed to speed up the addition operation by adding a propagation of carry bit around a portion of entire adder.
Fig. 2 shows the architecture of CSkA.

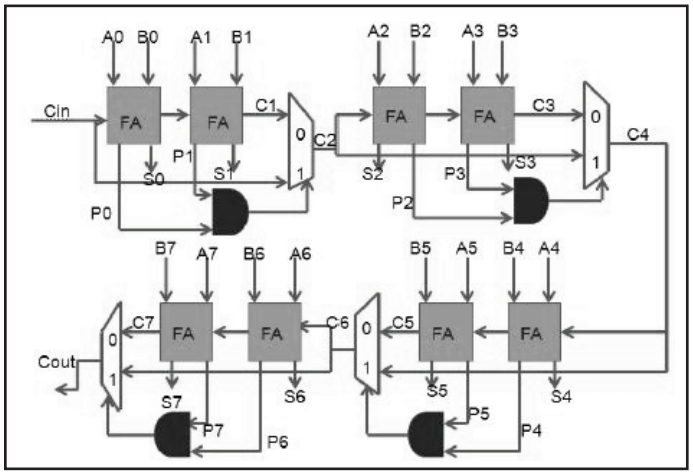

Fig. 2(a): Block Diagram of CSka

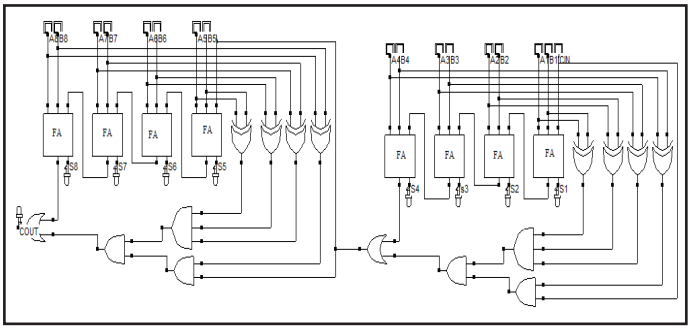

Fig. 2(b): Schematic of Carry Skip Adder

The carry-in bit designated as Ci. The output of RCA (the last stage) is Ci+4. The Carry Skip circuitry consists of two logic gates. AND gate accepts the carry-in bit and compares it with the group of propagated signals [2] given below.

$$P_{[i,i+3]} = (P_{i+3})*(P_{i+2})*(P_{i+1})*P_i \quad (1)$$

$$\text{Carry} = C_{i+4} + (P_{[i,\,i+3]})* C_i \quad (2)$$

C. Carry Increment Adder

The design of Carry Increment Adder (CIA) consists of RCA's and incremental circuitry [1]. The incremental circuit can be designed using HA's in ripple carry chain with a sequential order. The addition operation is done by dividing total number of bits in to group of 4bits and addition operation is done using several 4bit RCA's. The architecture of CIA is shown in fig. 3.

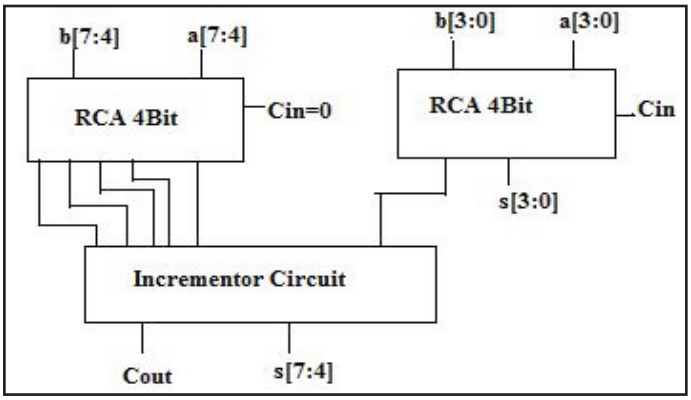

Fig. 3(a): Block Diagram of CIA

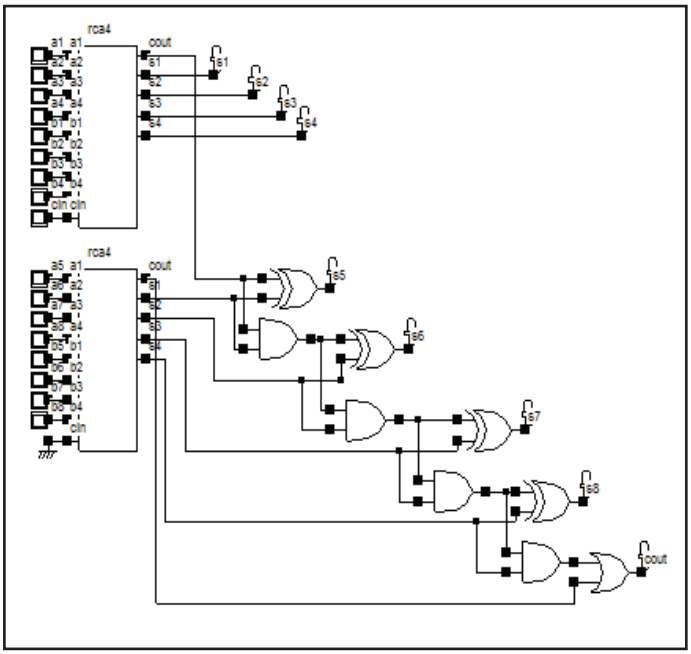

Fig. 3(b): Schematic of CIA

D. Carry Look Ahead Adder

Carry Look Ahead (CLA) design is based on the principle of looking at lower adder bits of argument and addend if higher orders carry generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate [2]. As shown in fig. 4(a), in the generation and propagation stage, the generation values, propagation values are computed. Internal carry generation is calculated in second stage.

And in final stage, the sum is calculated. The flow chart of CLA is given in fig. 4(a) and the architecture of CLA is given in fig. 4(b) and fig. 4(c).

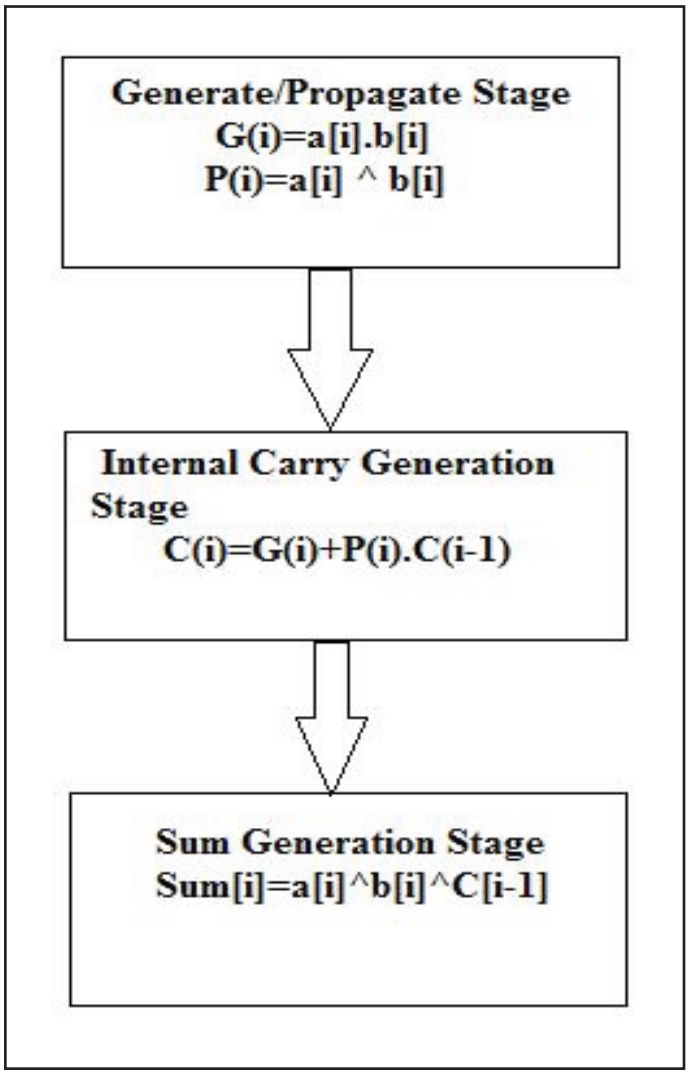

Fig. 4(a): Flow chart of CLA

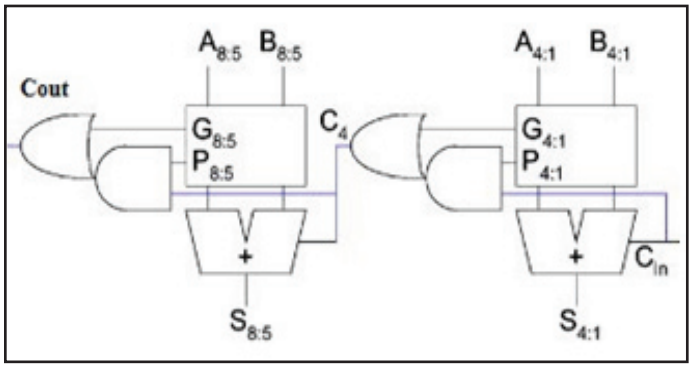

Fig. 4(b): Block Diagram of CSLA

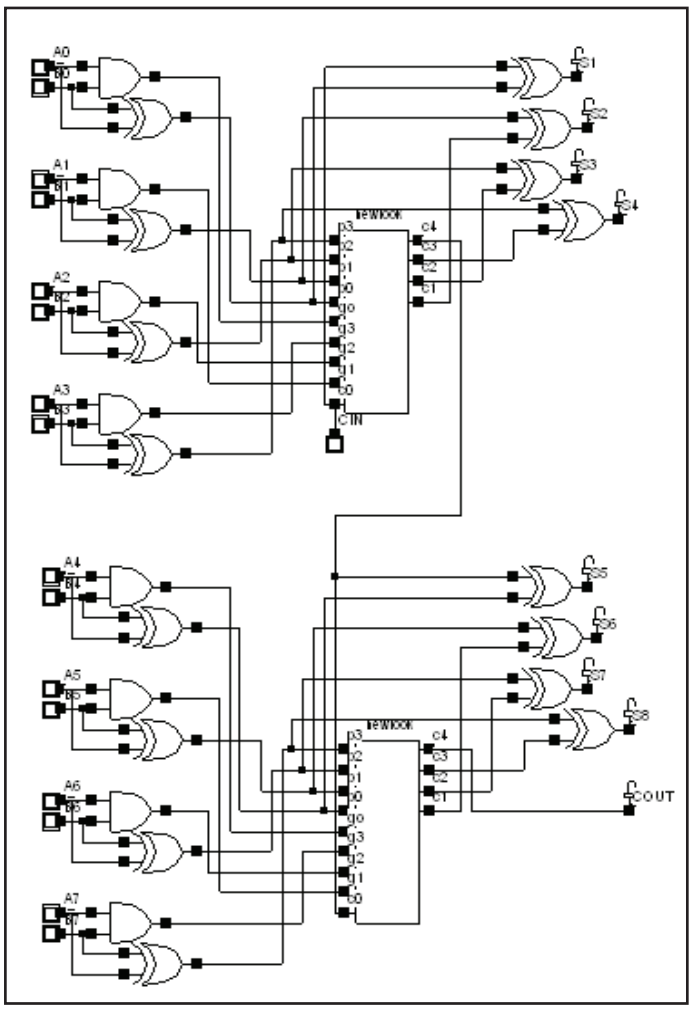

Fig. 4(c): Schematic of CSLA

E. Carry Save Adder

In Carry Save Adder (CSA), three bits are added parallelly at a time. In this scheme, the carry is not propagated through the stages. Instead, carry is stored in present stage, and updated as addend value in the next stage [2]. Hence, the delay due to the carry is reduced in this scheme.

The architecture of CSA is shown in fig. 5.

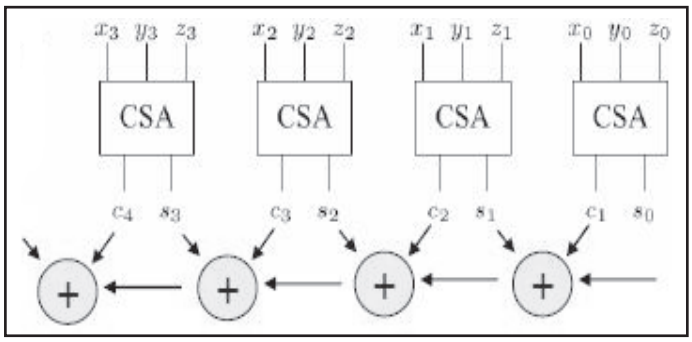

Fig. 5(a): Block Diagram of CSA

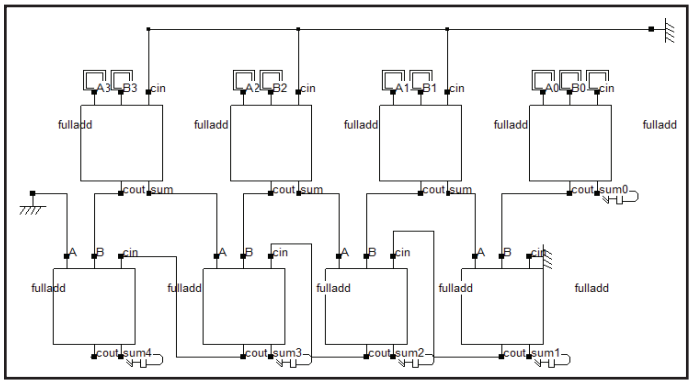

Fig. 5(b): Schematic of CSA

F. Carry Select Adder

Carry Select Adder (CSlA) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 are executed parallelly [14]. Depending upon Cin, the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected. Hence, the delay is reduced.

However, the structure is increased due to the complexity of multiplexers [4]. The architecture of CSlA is illustrated in fig. 6.

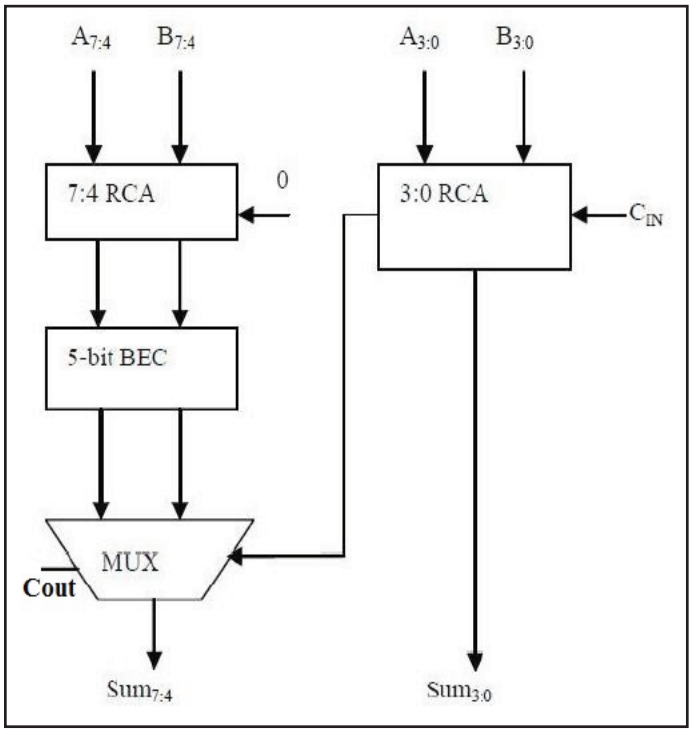

Fig. 6(a): Block Diagram of CSlA

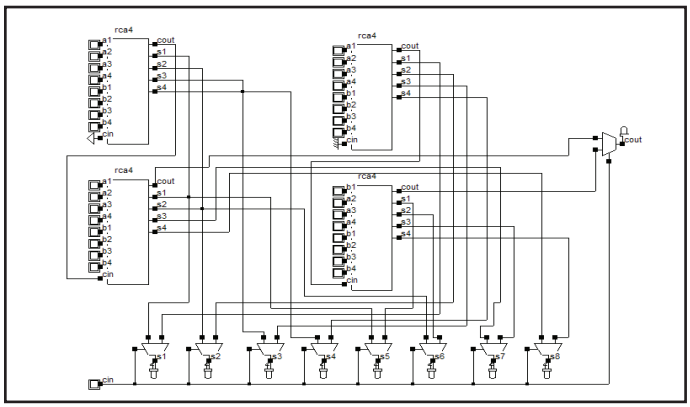

Fig. 6(b): Schematic of CSlA

G. Carry Bypass Adder

In Carry Bypass Adder (CBA), RCA is used to add 4-bits at a time and the carry generated will be propagated to next stage with help of multiplexer using select input as Bypass logic. By pass logic is formed from the product values as it is calculated in the CLA. Depending on the carry value and by pass logic, the carry is propagated to the next stage [1].

The architecture of CBA is given in fig. 7.

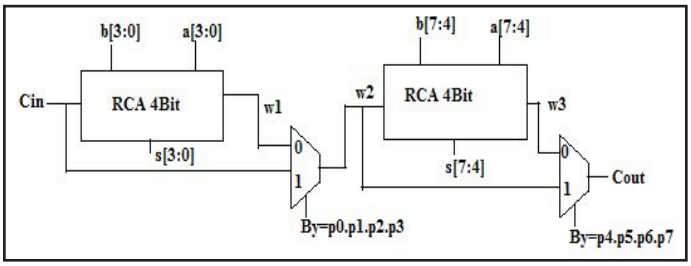

Fig. 7(a): Block Diagram of CBA

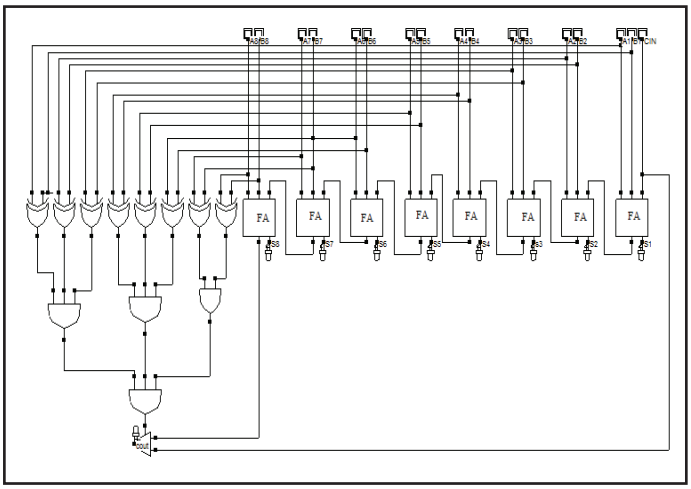

Fig. 7(b): Schematic of CBA

III. Comparison

The performances of adder topologies are discussed for robustness against area, delay and power dissipation [1]. They are selected for this work since they have been commonly used in many applications. Addition is an indispensable operation for any high speed digital system, digital signal processing or control system. Therefore pertinent choice of adder topologies is an essential importance in the design of VLSI integrated circuits for high speed and high performance CMOS circuits. With operating frequency of 500MHz, power dissipation, area, gate count and delay for all adder topologies discussed earlier are observed.

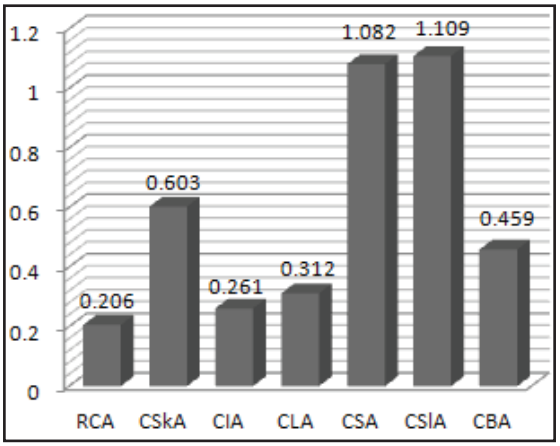

Fig. 8: Power (in mW) Distribution Graph

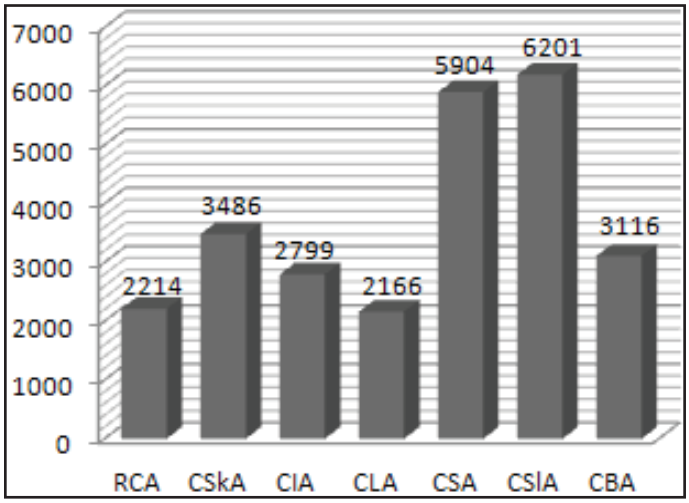

Fig. 9: Area (in µm2) Distribution Graph

From the power distribution graph shown in fig. 8, it is observed that the maximum power dissipation occurs for carry select adder and next comes the carry save adder. The least power dissipation occurs for ripple carry adder and carry increment adders. From the area distribution shown in fig. 9 and gate count shown in fig.10, the carry select and carry save adders occupies more area and gate count, ripple carry and carry increment occupies less area and gate count. From fig. 11, it can be observed that ripple carry adder is slowest adder among all other.

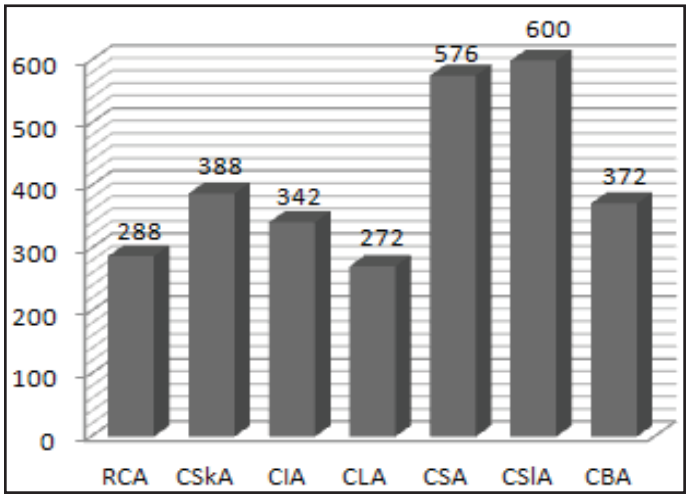

Fig. 10: Gate Count Graph

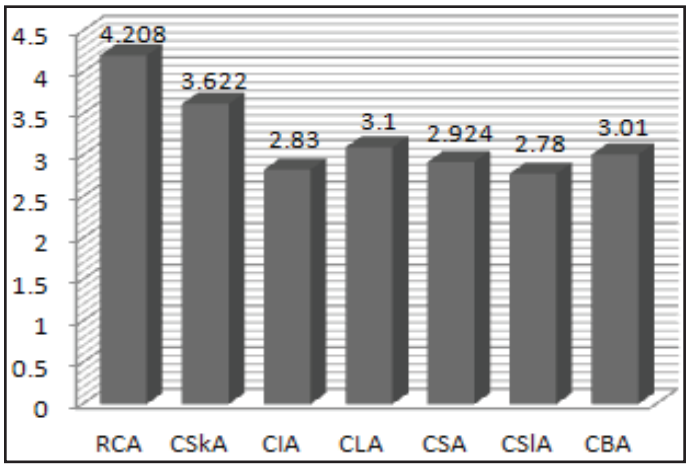

Fig. 11: Graph for Delay (in ns)

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