A Review on Ultra Low Power Design Technique: Subthreshold Logic

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Abstract
Rapid increases in chip complexity, increasingly faster clocks and proliferation of portable devices have combined to make power dissipation an important design parameter. The power consumption of a system determines its heat dissipation as well as battery life. For some digital systems, power consumption has become the most critical design constraint. To satisfy the low power requirement one of the best technique sub-threshold logic is being introduced. This paper presents a complete review of recent research and explores all aspects/ constraints of subthreshold logic design technique. The paper explores basics of subthreshold, sources of power dissipation, challenges in subthreshold design, optimization methodology and various types of techniques which are currently used to implement ultra low power based circuits using subthreshold logic.

Keywords
Subthreshold, DIBL Leakage, MTCMOS, PVT Variations, RSCE

I. Introduction

In many applications ultra low Power based circuit design has become a primary design metric for manufactures. Due to technological advancement, power reduction is highest in jurisdiction when compared to speed and performance. Higher Power consumption increases the on-chip temperature which results in reduced operating life of the chip and battery life [1-5]. To satisfy the low power requirement of the CMOS based circuits, sub-threshold logic is being introduced which involves scaling voltage below the device threshold [6]. Extensive research is going on the subjects of sub/near-threshold digital design and their challenges, the goal of this paper however is to cover a border range of subthreshold based digital system designs, to show the interrelation of different solutions and their effective methods for low power digital design and review the recent updates and new advances in ultra low power era [8].

As the whole logic core of chip operates at a power supply falling from nominal level to the value less than threshold of MOS transistor i.e. ($Vdd < V_t$), the power dissipation can greatly be reduced according to the square law dependence on the supply voltage, however the penalty of speed degradation is also obvious. Despite fabricated in deep submicron CMOS technologies, when MOS transistor in the circuits are forced to operate in subthreshold region (weak inversion region), the drain to source ON current can drop much lower than 100 nA, resulting in ultra low frequency. All the MOS transistors which operate in the weak inversion region will have a very small amount of subthreshold leakage current, which is utilized as conduction current to obtain the ultra-low power consumption. Equation (1) shows that subthreshold leakage current is exponentially dependent on V_t hence it increases with decrease in V_t [1].

$$I_{leak} = I_0 e^{\frac{V_{GS}-V_{th}}{nV_T}}\left(1-e^{-\frac{V_{DS}}{V_T}}\right) \quad (1)$$

Where

$$I_0 = \mu_0 C_{ox}\frac{W}{L}V_{th}^{\ 2}e^{1.8}$$

The subthreshold leakage current is also exponentially related to the gate voltage. This exponential relationship is expected to give an exponential reduction in power consumption, but also an exponential increase in delay. Thus more leakage currents and more dissipation of heat increases the on-chip temperatures which cause more power dissipation [7]. Decreased Vt leads to the exponential increase in the subthreshold leakage current and hence increases leakage power. These types of trade-offs ultimately mean that the problem facing process and circuit engineering become more complicated with each generation [9]. In the present scenario more than 50% power dissipation occurs due to leakage current to the entire chip [10], Hence Sub-threshold design approaches are appealing for a wide range of low power or energy applications.

II. Sources of Power Dissipation

Power consumption has become a primary constraint in VLSI design. Several methodologies, energy efficient algorithms, logic families has already been invented which directly addresses power reduction, with the focus rather on ever faster clock rates and logic speeds in subthreshold design technique. How to get more reduction efficiently to design a robust circuitry in subthreshold region is the main focusing area for researchers in both industry and academia. The approach which will be presented here, takes another viewpoint, in which all possible power constraints and their types of a CMOS based system design are investigated with the goal of the reduction in the power dissipation [11].

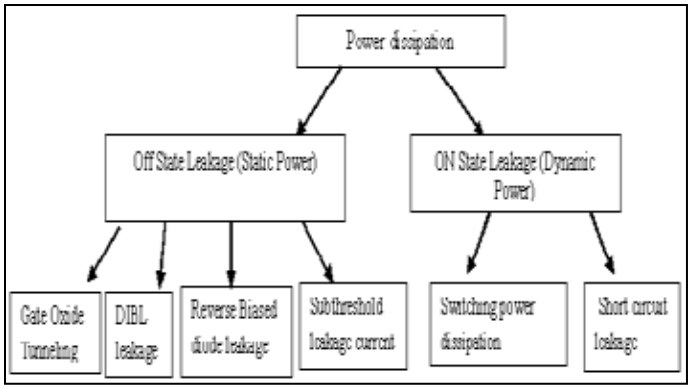

Fig. 1: Main Sources of Power Dissipation in CMOS

Power consumption is an important property of a design that affects feasibility cost and reliability. It influence a greater number of critical design decisions, such as power supply capacity, the battery lifetime, supply line sizing, packaging and cooling requirements. Fig1 shows the main constraints of power dissipation and their types in CMOS based VLSI design circuits. There are three major sources of power dissipation in digital CMOS circuits which are summarized in the following equation (11)

$$P_{avg} = P_{switching} + P_{shortcircuit} + P_{leakage} \quad (2)$$
$$\alpha_{0-1} \cdot C_L \cdot V_{dd}^2 \cdot f_{clk} + I_{sc} \cdot V_{dd} + I_{leakage} \cdot V_{dd}$$

The first term represents the switching component of power, where C_L is the load capacitance; f_{clk} is the clock frequency and $\alpha_{0-1}$is the probability that a power consuming transition occurs (the activity factor).

The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Short circuit leakage depends on the supply voltage, device threshold, the input rise/fall time and the operating frequency of the transistor. In the absence of the load the maximum short-circuit current flows, short circuit is negligible at subthreshold.

These first two terms in eq (2) comes in the category of dynamic power dissipation (ON state leakage) which are the main component of power consumption as shown in fig. 1. It occurs by charging and discharging of the various load capacitances and short circuit current during ON state condition of the transistor. As the supply voltage is reduced below the threshold voltage huge amount of dynamic power reduction is achieved because of the quadratic influence. At subthreshold, switching current is much greater than leakage current hence dynamic power have great impact of the overall power consumption as compare to leakage current.

The last term in eq (2) is leakage current, Ileakage, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. Moreover the power consumed by the subthreshold currents and by reverse biased diodes in a CMOS transistor is considered as leakage power or off state leakage power (static power). The leakage power of a CMOS logic gate does not depend on the input transition or load capacitance. It remains constant for a logic cell. Leakage component in bulk CMOS is categorized as diode reverse bias current or reverse biased, drain and source substrate junction band to band tunneling, subthreshold current, gate induced drain leakage and gate oxide tunneling as shown in fig. 1.

Since the focusing constraints of this review paper is subthreshold leakage so we will describe broadly. The subthreshold current always flow from source to drain even if Vgs is lesser than Vth of the device. This happened due to carrier diffusion between source and drain regions of the CMOS transistor in weak inversion. The subthreshold current become significant current Isub, which occurs when Vgs is below Vth, is the main part of the leakage current. It has also been investigated that off state current occurs due to gate leakage near the drain region of the device and experimental manipulation states that it increases with the increments in number of transistors of the chip. It is estimated that the silicon oxide can scale down to the 1.4 to 1.5 nm regime for high performance application. The off-state leakage will remain within the target specifications (nA/ m). However for low power application gate leakage dominates the gate oxide issues with respect to scaling silicon oxides, for that oxide thickness may be limited to 1.8 to 2.0 nm regime with the reduction of the off-state power consumption and maintain an acceptable level of charge retention. Reliability will probably limit silicon oxide scaling for high performance applications whereas gate leakage will limit gate oxide scaling for low power and memory applications [12]. Direct tunneling phenomena of the discrete charges randomly crossing a potential barrier in the gate oxide thickness produces a non-negligible gate current. This leakage current is the main source of the static power consumption for digital circuits [13]. W.Kirklen et.al. describes about the significant consequences of the off-state leakage which occurs due to short channel effects in sub-100 nm CMOS technology. The surface punch through conduction mechanisms arises DIBL leakage characteristics and the main dominant constraints for these leakages are channel length, drain bias and temperature, whereas the main constraints for gate leakage currents are oxide thickness and gate bias. Antoni Fer et. al. studied about the subthreshold leakage current and their effect of the variation in the threshold voltage due to short-channel effects and statistical variations of long channel threshold voltages due to doping, Author presents a statistically characterized model which is based on the subthreshold leakage at transistor and cell level and obtained the leakage power consumption of a standard cell circuit , concluded that IC having short channel length and high power leakage will be faster and vice versa than the nominal ones [14].

III. Challenges in Subthreshold Design

The main goal of this section is to focus on the challenges of subthreshold logic design; the characteristics of the semiconductor behavior vary in weak inversion. The minimum power supply, frequency reduction and many others challenging parameters will be discussed in the following [15-18]

A. Delay

The first and preeminent challenges of the circuit operation in the subthreshold region are the longer impediment or delay relatively having lower frequency due to weak current flow in the channel.

B. Device Scaling

The device scaling provides great merits like reduction in gate capacitance, switching energy and gate delay. On the other hand there are some demerits like including process variability, increased subthreshold leakage, increased gate leakage at super-threshold voltages, exponential sensitivities to V th, Vdd, and inverse subthreshold slope. Transistor design is important in case of subthreshold regime and these days researchers are trying to find out how subthreshold circuits will fare under device scaling and to provide improved scaling strategies targeting the needs of subthreshold circuits.

C. Exploring New Logic Families for Robust Design

The current ratio ION/IOFF decreases with low Vdd which may reduce robustness due to this reason static CMOS gates works continuous and gives better results in subthreshold but because of scaling, voltage or process variation and other arising effects CMOS offer greater resiliency. A lot of work needs to be done for exploring new logic families to design a robust subthreshold logic circuits.

D. PVT Variations

Process, Voltage, and Temperature (PVT) variations substantially affect the threshold voltages and frequency which causes a large variance in the behavior of subthreshold circuits, just because of exponential I-V characteristics, threshold voltage variations occurs due random dopant fluctuations and they change the properties of a transistor relative to its immediate neighbors . These signal delay variations can lead to timing violations. Therefore variability-aware design is an important challenge for robust and reliable subthreshold circuits.

E. Temperature

The effect of temperature variation on the circuit behavior is another important challenge, mobility degradation in the channel during strong inversion generally slow down the circuit and also rises the temperature. This arising temperature decreases threshold voltage which exponentially increases subthreshold current. In other term we can say when temperature scaling is performed the circuit gets cool down it not only increases mobility but also minimizes subthreshold leakage. Generally at low temperature gate leakage becomes the main leakage.

F. Advancement in Design Tools

System verification is a significant task after designing. With the advancement of technology, design tools modification must be done having the additional function like statistical distributions of delay and power, introduced by local variations so that verification of large systems running at such ultra low voltages and power dissipation estimation of circuits could be performed easily.

G. Noise Margin

Noise margin is directly affected from the supply voltage and degraded due to the high sensitivity to process variations and low-Vdd subthreshold circuits. Therefore in the presence of noise special techniques must be used to design a subthreshold circuit.

H. Reliability Problems

Reliability failures are typically caused by marginal manufacturing defects that are not significant enough to prevent the IC from passing a production test but can cause failure under use. Test coverage problems and circuit sensitivity are always followed by reliability problem. Reliability problems are worst kind of problems due to potentially severe consequences.

IV. Design Optimization Methodology and Techniques for Subthreshold Operation

Design optimization methodologies are the application of numerical algorithms and techniques to engineering systems to assist the designers in improving the system's performance, weight, reliability, and/or cost. It can be applied during the product development stage to ensure that the finished design will have the high performance, high reliability, low weight, and/or low cost. Moreover to achieve a cost effective, less energy dissipation, low device capacitance, high drive current, good sub-threshold swing, less sensitive to random dopant fluctuations, reliable circuits various techniques and circuit design methodology have been developed. Since the gradual change of characteristics with passage of time in transistor causes a circuit variability like hot carrier injection (HCI), bias temperature instability (BTI), and time dependent dielectric breakdown (TDDB), Negative bias temperature instability(NBTI) have become more prevalent issues. These different circuit variation occurs when a transistor is held in the 'on' state as HCI occurs due to the existence of high electric field in the channel near drain region, BTI usually happens due to the interface traps at the channel-oxide interface, TDDB take place due to catastrophic failure because defects pile up and a short circuit forms occurs inside the oxide layer with high electric field and the last variable NBTI occurs due to positive shift in the absolute value of the PMOS threshold voltage, increment in the threshold voltage consequent decrease in drain current and transconductance, Various circuit techniques have been developed to address these issues. To overcome the problem of all these issues the main goal of this section is to describe a variety of existing design methodologies and techniques at circuit level as well as device level leakage reduction.

A. Circuit-Level Optimization Methodologies for Subthreshold Operation

Today's latest research area is to develop novel circuit technology to reduced subthreshold leakage current with minimum power consumption. There are so many existing circuit techniques have already been developed to turn off these leakage currents. As technology continues to scale exponentially subthreshold leakage current is become a main concern of reduction. In general source biasing and direct threshold voltage (Vt) manipulation is the main approach for high performance and low leakage requirements in the circuit level.

1. Source Biasing

The source biasing is mainly used to control the leakage current during standby modes, in this a additional positive voltage is applied to the source terminal of an off device which reduces subthreshold leakage current because Vgs voltage become negative due to body effect arises between a gate's source nodes and ground. The switched source impedance concept and self reverse biasing mechanism is popular to generate the biased source voltage. In switched source impedance a passive resister is switched in between a gate's source nodes and ground during standby mode and during active mode this degenerating resister is bypass to ground, but a large value resistor is used and its placement depends on knowing the standby state of every gate so these circuits are rarely used. In self reverse biasing mechanism standby leakage is controlled by using transistor stacks means subthreshold leakage current which flows through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off [19-20].

2. Multiple V_{th} Designs

In Multiple-threshold CMOS technologies both high and low-threshold transistors is implemented in a single chip which suppresses the subthreshold leakage current. A high performance circuit is achieved by inserting high-threshold devices in series to low Vth circuitry, in active mode operation high Vth appears to performing a circuit operation, whereas in standby mode one high Vth is to be appeared in each path from power to ground for leakage current reduction. Multiple Vth Designs can be achieved by adjusting the channel doping densities which required two additional masks, multiple gate oxide CMOS (Mox CMOS), multiple body bias and multiple channel length due to direct proportionality of threshold voltage to channel length . Generally longer channel lengths having high threshold transistors increase the gate capacitance, which has negative effect on performance and power. So short-channel transistors are better and mostly used. So following developing techniques is used to design a multiple-threshold circuit.

(i). Dual Threshold CMOS

Dual Vth technique uses two threshold voltages like in noncritical paths higher threshold voltage is assigned whereas in critical path low threshold transistor is to be used in a special logic design style like domino logic circuits for leakage power reduction during both standby and active modes without delay and area overhead, but it has become more complicated design time and the inability to stop critical path leakage during standby mode.

(ii). Variable Threshold CMOS

To achieve a variable threshold voltage a self substrate body-biasing is used to control the body bias , generally body bias is zero in active mode whereas in standby mode a deeper reverse body bias is applied to achieve highly threshold voltage and cut off the leakage current.

(iii). Dynamic Threshold CMOS

By making the connection between the gate and body together forms a dynamic threshold CMOS.DTMOS can be developed in triple wells of bulk silicon technology. Dynamic threshold voltage employ a back- gate bias control signals for power savings and active leakage power reduction. Diode built-in potential between source and drain should be reverse biased that limits the supply voltage. So this can used for ultralow power voltage circuits in bulk CMOS.

(iv). Sleep Transistor Sizing

A sleep control scheme is introduced for efficient power management, in standby mode small sleep devices further reduces leakage current but in active mode small sleep devices sink less current through to ground so its switching speed gets slow down, due to these constraints bouncing created at the virtual rails and effectively pinches VDS for the low Vth circuit.

3. BGMOS and SCCMOS

The effectiveness of MTCMOS sleep transistors increases by using two approach boosted gate MOS (BGMOS) approach and super cut-off CMOS (SCCMOS)

The BGMOS suggests that overdriving the gate voltage of sleep devices in active mode can reduce the area devoted to sleep devices, this overdriven (above Vdd) gate voltage make able a smaller device to sink the required amount of current in active mode while still effectively stemming the leakage current in standby mode. A similar approach called Super Cut-off CMOS (SCCMOS) advocates under driving gate voltages in standby mode For example, an NMOS sleep device would be turned off in standby mode with a negative gate voltage rather than a gate voltage of 0 volts.

4. Supply Voltage Scaling

Supply voltage scaling is very promising and efficient method for switching power reduction, gate leakage and subthreshold leakage power due to quadratic dependence of the switching power on the supply voltage and DIBL decreases as the supply voltage is scaled down.

5. Embedded Multi-Vth CMOS Design (Static Approach)

The static approach does not employ any control signals as dynamic techniques employed. In this technique a low Vth is to be provided for a several balanced critical path components and for noncritical path component high Vth is to be provided for maintain high performance low power circuit topologies. But in embedded multi- Vth some non critical gates become a critical gates after providing a high Vth this is the one of the disadvantage associated with it [18].

B. Device-Level Optimization Methodologies for Subthreshold Operation

Device-level optimization methodologies giving a good insight for subthreshold operation specially to optimize the channel profile which minimize the off-state leakage while maximizing the linear and saturated drive currents for high performance and low leakage requirements in upcoming future technology nodes. Device-level optimization focus on the new developing technology which having high-resolution lithographic techniques, new device designs, optimized gate oxide thickness , junction scaling , structures, and many more to keep the most undesirable short channel effects (occurs due to high drain voltage and reduced gate threshold voltage at which the device turns on) under control at very small dimensions. To keep these facts following major process techniques has been developed for leakage control and reduction at device level.

1. Device level Optimization Methodology in Bulk CMOS

There are a lots of string parameters exist in bulk CMOS which directly effects the performance of the device so to operate a device in a subthreshold region following changes can be possible in bulk CMOS.

(i). Changes in Channel Doping Profile

Channel doping profile like halo (near the source-substrate and the drain-substrate regions) and retrograde doping is very important aspect in super-threshold transistor to suppress the undesired effects like short- channel effects and also reduces the drain-induced barrier lowering (DIBL), prevent body punch through and control the threshold voltage of the device independent of its subthreshold slope. But these kinds of undesirable affects are very low in low bias subthreshold operation so halo and retrograde doping are not necessary. Due to the absence of these doping profile in subthreshold operation a significant reduction of the bottom junction capacitances is achieved which also reduces switching power, the delay of the logic gates, reduce substrate noise effects and parasitic latch-up. So it is essential to have low doping level in the bulk of the device for a significant subthreshold operation.

(ii). Changes in Oxide Thickness

Oxide thickness is very essential parameters to improve subthreshold slope, minimum oxide thickness does not guarantee minimum energy consumption, since optimized Tox minimizes the effective gate capacitance Cg. Specifically reducing Tox improves subthreshold swing S; it however, also increases Cg. Therefore, it is demonstrated that minimizing oxide thickness to improve subthreshold slope does not necessarily so in case of subthreshold oxide thickness will be optimized considering the changes in both transistor effective capacitance and the subthreshold slope to achieve minimum power consumption

2. Optimization Based on Subthreshold Logical Effort

Logical effort is also one of the major concern in device level optimization methodology for subthreshold operation, it depends on mobility difference between the carriers between the PMOS and NMOS devices. The optimal ratio of PMOS width and NMOS width Wp:Wn should be approximately 2.5:1 for achieving equivalent current drivability.

(i). New Device Sizing Utilizing Reverse Short-Channel Effects

Device-size optimization method utilizing reverse short-channel effect (RSCE) which is used to achieve high drive current, low device capacitance, less sensitivity to random dopant fluctuations, better sub-threshold swing, process variations, improved energy

dissipation and optimal performance in sub-threshold circuits. Due to very small amount of drain-to-source voltage SCE mechanism is not become so effective in subthreshold circuits as compare to super-threshold circuits ,moreover subthreshold current having an exponential function of Vth .RSCE has brought a significant impact on subthreshold performance. However, RSCE becomes more significant with process scaling due to the Retrograde Doping and Halo Doping, since this RSCE uses longer channel-length devices having not any impact on the load capacitance, improves drive current and their threshold voltage decreases as the channel length increases so the combination of SCE and RSCE causes the Vth to peak at a channel length slightly longer than the minimum value in super-threshold devices.

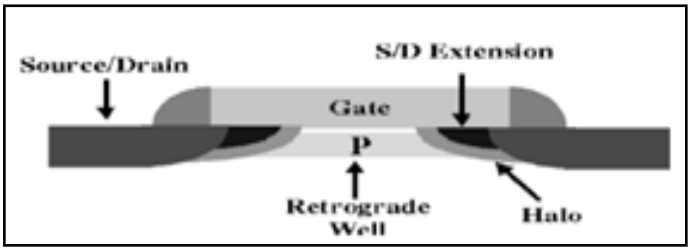

Fig. 2: Graphical Representation of Different Aspects of Well Engineering [42]

An increment in Channel doping concentration profile like halo doping (nonuniform channel in a lateral direction) and retrograde doping(vertically nonuniform, low-high channel doping) as shown in fig provide a excellent way to control the dependence of threshold voltage on channel length , SCEs , drain-induced barrier lowering (DIBL), prevent body punch through in low bias subthreshold operation. In halo doping for an n-channel MOSFETs, more highly p-type doped regions are introduced near the two ends of the channel. This highly doped regions consume a larger fraction of the total channel, also reduces charge-sharing with the threshold voltage degradation with respect to the reduction of channel length, since this threshold voltage does not depend on channel length hence the off-current becomes less sensitive to channel length variation, on channel length becomes more flat Hence, the off-current becomes less sensitive to channel length variation. The reduction in drain and source junction depletion region width also reduces the barrier lowering in the channel, thus reducing DIBL. Since the channel edges are more heavily doped and junction depletion widths are smaller, the distance between source and drain depletion regions is larger. This reduces the punch through possibility.

C. Double-Gate Dynamic Threshold SOI CMOS (DGDTMOS)

When the advantages of DTMOS and double-gate FD SOI MOSFETs combines together forms a new technique called asymmetrical double-gate dynamic threshold voltage (DGDT) SOI MOSFET without any limitation on the supply voltage. As name suggest the thin fully depleted silicon body sandwiched between two gates provides excellent gate control over the channel, to get large threshold voltage than supply voltage. Back-gate oxide is basically thick as compare to front gate, surface potential of both gate are strongly coupled and dynamically dependent to each other. The double gate provides better scalability and optimized device characteristics including ION and IOFF compared to bulk CMOS.

Various DGMOS device optimization methodologies for subthreshold operation have been identified that are presented in the following subsections

1. DGMOS Devices with Optimum Longer Channel Lengths and Simplified S/D Structure

Basically long-channel device will be more suitable in subthreshold operation than short-channel devices due to dependence of delay on gate length which is mainly decided by Cg, when velocity saturation occurs, ION is a weak function of gate length. Delay increases linearly with the increase of gate length in super-threshold operations. So, long-channel device will be more suitable more subthreshold operation than short-channel devices.

2. DGMOS Devices with Optimum Underlap for Subthreshold Operation

Due to optimum gate underlap a significantly reduction in the parasitic fringe (Cfr) and overlap(Cov) capacitances which strongly depends on the device geometry of DGMOS is to be analyzed resulting with high performance and lower power consumption , but in reality , in an underlap device there is no Cov, the effective gate capacitance (Cg) is dominated by Cfr.

DGSOI Technology with Codesign Methodology for Optimal Subthreshold Operation: Since the conventional design techniques are not optimal for subthreshold design. After many demonstration double gate MOSFETs are better suited for subthreshold operation (~10× higher throughput at iso-power) and gives significant improvement in PDP than bulk MOSFETs just for having only reason that DG -SOI has no intrinsic capacitance in the subthreshold region.

Carbon Nanotube (CNFETs) Technology for Subthreshold Operation: An Aggressive scaling of CMOS devices has exponential increase in leakage current and large parameter variations , hence researcher brings to focus on a alternative devices and circuit architecture in a sub-10-nm transistor era as Carbon nanotube field-effect transistors (CNTFETs) have been consider as a complement of future semiconductor devices due to high mobility, low defect structure, and intrinsic nanometer scale of carbon nanotubes (CNTs). CNTs are sheets of graphite rolled in the shape of a tube.

V. Logic Families for Subthreshold Operations

A logic family is a collection of logic gates and a set of techniques which is used to implement logic within VLSI integrated circuits. Basically logic family uses static techniques to minimize a design complexity and to minimize size, power consumption, and delay domino logic which uses clocked dynamic techniques. The main goal of this section is to cover all types of logic families which is used to implement a high speed, low power, reliability (based on noise margins), and good compromise between high speed and ultra-low power design for designing optimal subthreshold operation. One challenge with subthreshold operation is that the transistor drive currents are exponentially related to the threshold voltage, rather than linear to quadratic as in superthreshold operation and this can lead to pull-up / pull-down mismatches. An elegant solution was proposed to this sensitivity and is referred to as self-adjusting threshold logic. Depending on the parameter like speed, robustness, power etc a several different logic style exists to implement a same kind of chip in subthreshold operation [21]. The following logic families have been explored to design a more robust and energy efficient subthreshold circuits

A. Subthreshold CMOS Logic

Sub-CMOS logic is the conventional CMOS logic operated in the subthreshold region. The exponential relationship between Ids and Vgs in subthreshold region gives rise to an extremely high transconductance, gm. The much improved VTC yields better noise margins. Circuit designers can have more freedom in sizing the circuits and still obtain a near optimum delay value than strong inversion CMOS due to the wider range of flatness of PMOS to NMOS ratio, sensitivity to power supply variation has a significant negative impact on subthreshold circuit as the sensitivity of the gate delay due to Vdd variation increases with decreasing power supply value for subthreshold CMOS logic. Hence, Vdd stabilization is crucial for the proper operation of subthreshold circuit [15].

B. Sub Domino/Dynamic Logic

It has excellent noise margin ,higher frequency of operation, lower power consumption, smaller area, better speed comparatively with the Sub-CMOS logic operating in subthreshold region. Therefore it is more efficient for ultra-low power applications. Table shows the comparison [22-23]

Table 1: Sub-CMOS Versus Subdomino Logic [15,22].

Parameter	Sub-CMOS	Subdomino
Power (nw)	10.64	3.408 (32%)
Delay (μs)	7.545	2.423 (3 × faster)
PDP (fJ)	80.28	8.26 (10%)
Area (μm²)	2381	1447 (60%)
Noise margins	poor	Excellent

C. Variable Threshold Voltage Subthreshold CMOS (VT-Sub-CMOS) Logic

VT-Sub-CMOS logic is sub-CMOS logic with an additional stabilization scheme which monitors any change in the transistor current due to temperature and process variations and provides an appropriate bias to the substrate. Any increase of the current above certain pre specified threshold value is thus reduced by an appropriate bias to the substrate. Both logic and stabilization circuits of VT-sub-CMOS work in the subthreshold region.

D. Subthreshold Dynamic Threshold Voltage Logic (Sub-DTMOS Logic)

In this style of logic, some nodes are required to hold their logic value as a charge stored on a capacitor. These nodes are not connected to their 'drivers' permanently. The 'driver' places the logic value on them, and is then disconnected from the node. Due to leakage etc., the logic value cannot be held indefinitely. Dynamic circuits therefore require a minimum clock frequency to operate correctly. Sub-DTMOS logic provides an alternative way to achieve the same stability with direct substrate biasing without using additional control circuitry as in the case of VT-sub-CMOS logic. Sub-DTMOS logic uses transistors whose gates are tied to their substrates. It reduces the design complexity, power consumption substantially and having higher gain. Thus, using DTMOS logic, we can operate the circuit at much higher frequency while still maintaining the same energy/switching with enhanced robustness compared to static CMOS [23].

Table 2: Change in Energy/ Switching [23]

Parameter	Strong inversion-CMOS	Sub-CMOS	VT-Sub-CMOS
V_{th} variations (±10%)	0.1–1.4%	34.7–96.2%	5–42.4%
Temperature variations (25–10°C)	28.2%	61.5%	33.7%

E. Differential Cascode Voltage Switch Pass Gate (DCVSPG) Logic

The architecture of logic family reduces internal capacitances and reduces the load on the previous stage, hence improves the performance, provides more reliable operation and reduces the power consumption. It performs better than CMOS in terms of energy per switching and EDP, and achieves comparable operation speed. By utilizing DCVSPG gates more energy efficient system can be implemented. Table 3 shows the DCVSPG logic and conventional CMOS based NAND2 AND NOR2 logic gates to Compare the maximum operating frequency and EDP

Table 3: Comparison of EDP and Max Frequency [24]

	EDP(10^{-21} JS)		*Max. Frequency (MHz)*	
	CMOS	*DCVSPG*	*CMOS*	*DCVSPG*
NAND2(VDD=0.30V)	*0.50*	*0.20*	*1.10*	*0.83*
NOR2(VDD= 0.30V)	*0.57*	*0.20*	*1.04*	*1.43*

F. Subthreshold Pseudo-NMOS Logic (Ratioed Logic)

In subthreshold region, Pseudo-NMOS logic is more robust than Pseudo-n NMOS logic in strong-inversion, as its VTC is more closer to the ideal curve and also the voltage levels swing rail-to-rail due to large gain in subthreshold region, and does not suffer from low logic level degradation problem as with the case of the strong inversion. It is comparable to CMOS in terms of power and robustness but with much less area, capacitance, improved performance and achieve some improvement in operating speed. In Pseudo-NMOS logic Careful sizing of PMOS to NMOS ratio is a necessary for functions correctly. In summary Pseudo nMOS for subthreshold has better PDP and comparable robustness to static CMOS in subthreshold region as shown in Table 4

Table 4: Subthreshold PSEUDO-NMOS With Subthreshold CMOS [25]

	CMOS		Pseudo-NMOS	
Logic	Power (W)	Delay (s)	Power (W)	Delay (s)
INV	4.886e-09	2.234e-07	3.186e-08	5.474e-08
NOR-4	6.064e-09	8.034e-07	3.187e-08	7.054e-08
NOR-8	6.852e-09	1.808e-06	3.187e-08	9.160e-08
NOR-16	7.815e-09	4.482e-06	3.187e-08	1.337e-07
Full Adder	4.691e-09	1.377e-06	2.306e-08	2.219e-07

G. Subthreshold Pass Transistor (PT) Logic

The terms Pass signals are expressed in terms of input signal or supply. In this logic a low-impedance path exists to both supply rails under all circumstances means having no static power consumption, bidirectional and ratioless characteristics. Pure PT logic is not regenerative-the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion).Threshold voltage drop causes static power consumption (may be weakly conducting forming a path from

Vdd to GND) and Vth increases of pass transistor due to body effect (VSB).In this topology voltage drop does not exceed Vth when there are multiple transistors in the path. Demerit of the pass-transistor logic degrades as the voltages are reduced [15, 26].

H. Subthreshold Dynamic Threshold PT (DTPT) Logic

As modulating the body bias adjust the threshold voltage dynamically having different on- and off-state values. Hence we can use dynamic threshold transistors whose gates are tied to the substrates forming the subthreshold dynamic threshold pass transistor (Sub-DTPT) for a pass transistor [15]. It has been observed that controlling the body bias provide substantial speed increase and that such techniques are useful over a large range of supply voltages. Also Sub-DTPT logic shows better stability to the temperature variation than the corresponding subPass Transistor logic, can be used for a broad range of supply voltages and combination of DTMOS and restoration can provide the best performance in low-power applications [27].

I. Subthreshold Complementary Pass-gate Logic(CPL)

This topology eliminates the p-MOS transistor form the pass gate network which reduces parasitic capacitances and increases Operating speed .In CPL circuit the overall noise immunity reduces and makes the transistor more susceptible to sub threshold conduction in the off mode due to threshold voltage reduction to about the zero voltage of n-MOS transistor in the pass gate network through threshold adjustments implants in order to eliminate the threshold voltage drop[28]. This logic family controls the delay variability which occurs due to supply variations. The major contribution of delay variability is the input transition time variation , also depend on the ratio of the supply the transistor threshold voltage, thus low-power designs and down-scaled technologies are expected to be more sensitive to delay variations and they are independent of the gate load capacitance (i.e. fan-out and wire parasitics)[29]

J. Subthreshold Differential Static Logic

Sub-threshold static and ratioed/domino logic have recently been proposed to satisfy the ultra-low power requirement in applications such as hearing aid, pace-maker, wearable wrist-watch computer etc, operated only at lower frequencies due to lower supply voltage [22]. Source Coupled Logic (SCL) is one of the most thriving logic styles in high speed and high resolution applications which improved the speed of MOS based circuits but having a high amount of power consumption due to constant current, which passes through the supply a differential static CMOS Logic (DSCL) introduced that has advantages of the SCL such as high speed , lower power consumption and switching noise reduction..

VI. Conclusion and Future Direction

CMOS based digital circuits using subthreshold logic consumes less energy for active operation and dissipates less leakage power than higher voltage alternatives, subthreshold circuits are ideal for application where performance is not critical but minimizing energy consumption is key. To further enhancement of the subthreshold operation in terms of performance and robustness the comparative studies has to be done and concluded that at device level bulk CMOS devices suffers a lots of problems in subthreshold design techniques as compare to double gate SOI devices and CNFETs. Whereas at circuit level Sub-Pseudo-NMOS, Sub-DTPT and Subdomino logics are best option for robust subthreshold operation with improved performance and better stability for PVT variations with reduced or comparable energy/ switching as compare to that of conventional static CMOS logic. The extensive exploration has been done in subthreshold based modules which suffered a lots of the "sub-threshold problems" during the implementation of the chip such as low performance, instability, test difficulties, and poor reliability and the effect of other specific parameters like process sensitivity, area overhead, Drain Induced Barrier Lowering (DIBL) has not been researched extensively. For the future implementation the effect of above mentioned parameters should be taken care comprehensively in one design module.

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